



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/172,553

10/14/1998

JAMES E. GREEN

2914.IUS

9441

7590

06/02/2004

JOSEPH A WALKOWSKI
TRASK BRITT & ROSSA
PO BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER

DIAZ, JOSE R

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application N .

09/172,553

Applicant(s)

GREEN ET AL.

Examiner

José R Díaz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 23 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 31-35 and 37-45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 31-35, 37-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 37-41 and 44-45 are still rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The claimed limitation structure comprising a HSG polysilicon layer on the storage poly and a dielectric material are not supported by Applicant's Specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

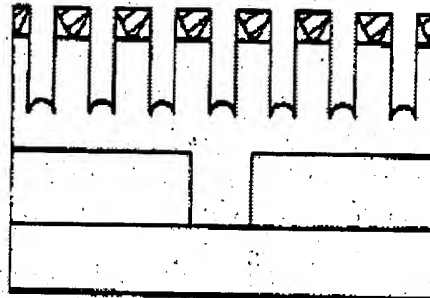
Claim 31-35 and 37-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Jun et al. (US Patent No. 5,256,587).

Art Unit: 2815

Regarding claims 31-32, 35 and 43, Jun et al. teaches an intermediate semiconductor capacitor structure (see figure 4c) comprising: a storage poly structure (13) comprising a plurality of contiguous mesas (consider the fingers or columns that include mask 15 and HSG 14 in fig 4c) with recess formed therein (consider the space between the fingers or columns in fig. 4c); a contiguous hemispherical-grain polysilicon (14) over said storage poly structure (13) (see fig. 4c) and a mask (15) over said hemispherical-grain polysilicon layer (14), said recesses (consider the space between the fingers or columns) being exposed through said contiguous hemispherical-grain polysilicon (14) and said mask (15) (see figure 4c).

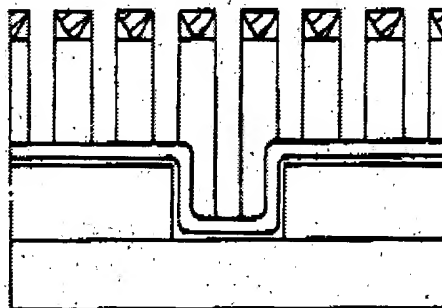
With regards to the terms "contiguous mesas" or "contiguous webs", please refer to figures 4c and 6c, below. Please note that figure 4c shows shallow recesses that do not disturb the continuity of the storage poly structure 13. Thus, figure 4c shows storage poly fingers connected throughout in an unbroken sequence.

F I G . 4c



By the contrary, figure 6C shows deep recesses that disturb the continuity of the fingers. Thus, in this case figure 6c does not show contiguous fingers. Therefore, the terms "contiguous mesas" or "contiguous webs" in view of Jun et al. will be define according to figure 4c, in which shallow recesses are provided without disturbing the continuity of the storage poly.

F I G . 6c



Regarding claims 33-34, 37 and 44-45, Jun et al. teaches an intermediate semiconductor capacitor structure (see fig. 4d) comprising: a storage poly structure (13) (see fig. 4d); a plurality of low contiguous elevation regions of a

Art Unit: 2815

hemispherical-grain polysilicon (14) on said storage poly structure (13) (see fig. 4d); recesses (consider the spaces between fingers or columns that are filled with layers 16 and 17) formed in said storage poly structure and located laterally between said low elevation regions of said hemispherical-grain polysilicon layer (14) (see fig. 4d); and a dielectric material (16) at least lining the recesses (see figure 4c).

Regarding claim 38, Jun et al. teaches an intermediate semiconductor capacitor structure (see figure 4d) comprising: a storage poly structure (13) (see fig. 4d); low elevation regions of a hemispherical-grain polysilicon (14) on said storage poly structure (13) (see fig. 4d); recesses (consider the spaces between fingers or columns that are filled with layers 16 and 17) formed in said storage poly structure (13) and located laterally between said low elevation regions of said hemispherical-grain polysilicon layer (14) (see figure 4d); and a dielectric material (16) substantially coating an upper surface of said storage poly structure (see top surface of the fingers or columns on which 14 is provided) (see fig. 4d) and lining each of said plurality of recesses (see figure 4d).

Regarding claim 39, Jun et al. teaches a cell poly structure (17) over the dielectric layer (16) (see figure 4d).

Regarding claim 40, Jun et al. teaches a web-like structure (consider the fingers or columns that include HSG 14 in fig 4c) comprising a plurality of contiguous top surfaces (please note that each finger or column includes at least two contiguous HSG triangles 14) (see fig. 4d).

Regarding claim 41, Jun et al. teaches that the recesses (consider the spaces between fingers or columns that are filled with layers 16 and 17) extend into said poly structure (13) (see fig. 4d).

Regarding claim 42, Jun et al. teaches an intermediate semiconductor capacitor structure (see fig. 4b) comprising: a storage poly structure (13) (see figure 4b); a substantially confluent HSG polysilicon layer (14) on said storage poly structure (13) (see figure 4b); and a mask (15) over said substantially confluent HSG polysilicon layer (14) (see figure 4b), elevated portions (top portion of the triangle) of said HSG polysilicon layer (14) being exposed through said mask (15) (see fig. 4b).

Response to Arguments

Regarding claims 31-34, Applicant's arguments have been considered but are moot in view of the new grounds of rejection.

Regarding claims 35, 37-45, Applicant's arguments filed February 23, 2004 have been fully considered but they are not persuasive.

35 U.S.C. 112, first paragraph

The specification does not disclose that a portion of the HSG polysilicon layer may remain covered by the mask such that some of the HSG layer will necessarily remain after the etch stop. Applicant has not provided any evidence that the disclosed process always necessarily results in some HSG remaining.

Art Unit: 2815

Applicant is reminded that a showing of obviousness --as opposed to inherency-- does not overcome a 112-first paragraph new-matter rejection.

35 U.S.C. 102(b)

Applicant argues that Jun does not anticipate the claimed invention since the HSG particles "appear to be quite separated from each other." (page 13 of Applicant's remarks). However, it seems that applicant has overlooked the express teaching disclosed in figure 4d of Jun in which "contiguous" HSG particles (14) are shown. As such, Jun anticipates the claimed limitation.

In addition, applicant also argues that Jun does not teach "a plurality of contiguous mesas" or "HSG having a web-like appearance." However, the examiner disagrees. On page 8 of Applicant's remarks, Applicant defined the terms "mesas" and "webs" as top surfaces of the storage poly. Based on such definition, Figure 22 (see below) shows, for example, top surfaces 1-9. It is noted that none of such "top surfaces" are contiguous as applicant argued. For instance, the "top surfaces" 1-8 are spaced apart from the main top surface 9.

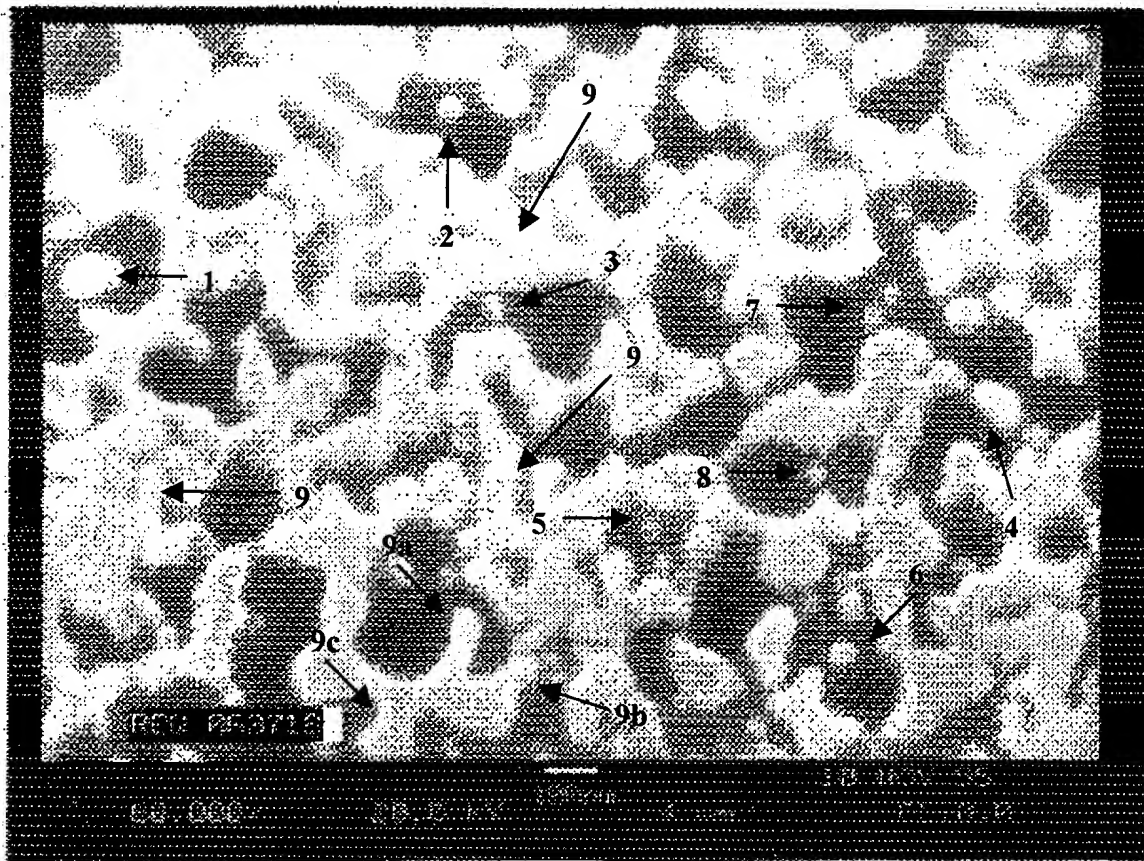


Fig. 22

Thus, the only two reasonable interpretations for the terms “contiguous mesas” and “contiguous webs” are:

First Interpretation

A mesa or web defined as a mere portion or region of a top surface. For example, the mesas or webs (fingers 9a-9c in figure 22, above) are “contiguous” because they share the same top surface (9).

Second Interpretation

The mesas or webs are contiguous by sharing the same base. For example, top surfaces A1 and A2 share base (B1); and A2 and A3 share base (B2), which is adjacent to base (B1) (see fig 9, below).

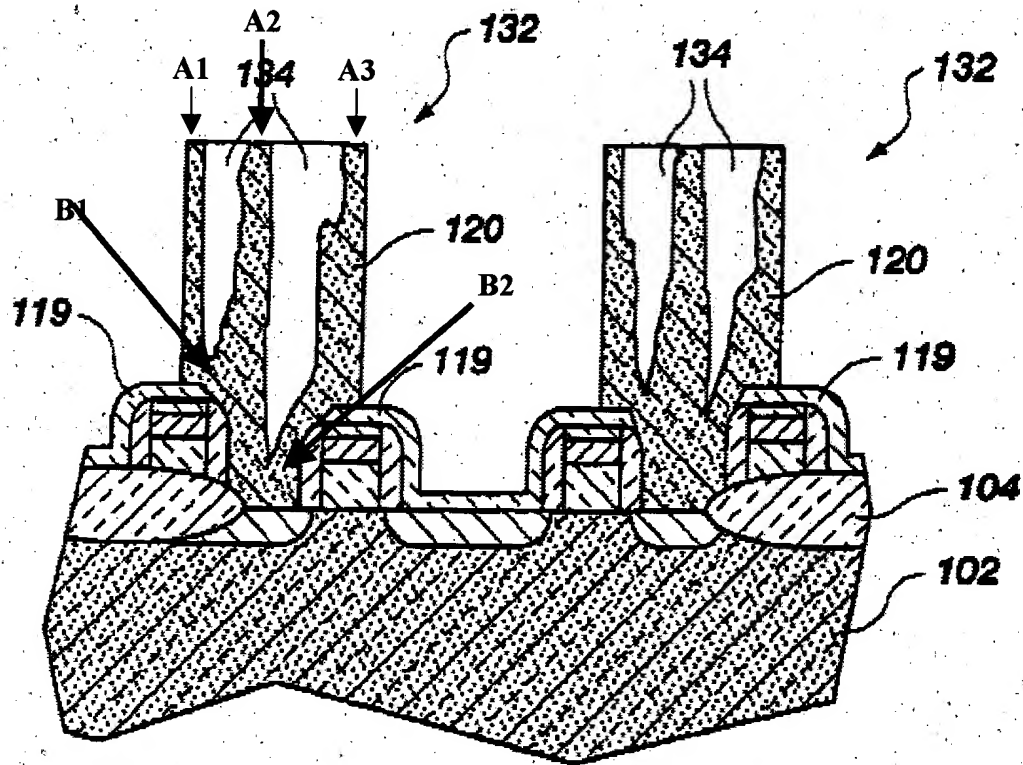


Fig. 9

Therefore, based on these interpretations it is believed that the reference Jun et al. anticipate the claimed invention. As such, the rejection under 35 U.S.C. 102(b) is considered to be proper.

Art Unit: 2815


Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
5/27/04


GEORGE ECKERT
PRIMARY EXAMINER